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Introduction

This document is prepared in the frame of the Tasks 6.2 “Outreach and Dissemination” and Task 6.3 “Exploitation” – (WP6).

Since ISOLDE is an open-source project, dissemination is essential for many reasons. Firstly, for maximizing impact: open-source projects thrive on collaboration and community engagement. Dissemination allows project outcomes and innovations to reach a wider audience, increasing the potential for adoption and utilization. By sharing knowledge, code, and documentation, open-source projects can have a broader impact and contribute to solving real-world problems. ISOLDE is aimed to build and contribute to the Reduced Instruction Set Computing (RISC)-V ecosystem in Europe, and although we have many stakeholders available in the project, outreach to external stakeholders is essential to reach maximum impact. This will also be done in close cooperation with the TRISTAN project which has similar ambitions. ISOLDE differentiates from TRISTAN by focusing on “stronger” application processors as to the “smaller” processors targeted by TRISTAN.

A well-designed dissemination approach will facilitate new collaborations. By making ISOLDE results publicly available, it becomes easier for others to contribute, provide feedback, and build upon the work done. This collaborative approach fosters innovation and accelerates the development of new ideas and solutions. Extension of the ISOLDE network to other stakeholders in open-source will help to increase the community and that will foster acceleration of innovations within ISOLDE.

Finally, we strongly believe that by getting feedbacks during dissemination activities from the RISC-V community, the quality and reliability of the IP blocks developed in ISOLDE will be improved. Although ISOLDE targets to achieve a Technology Readiness Level (TRL) 6, a large stakeholder community can help identify bugs, improve functionality, and enhance the overall quality and reliability of the project. This deliverable describes through the proposed dissemination plan the methodology and tools to be used to generate maximum dissemination impact.

Beyond dissemination, exploitation is also of crucial importance. Exploitation is a must-have to ensure that results end up in the market in a successful way. ISOLDE primarily aims to enhance and mature the European RISC-V eco-system and to support the ongoing shift towards open source methodologies and solutions in that context. Therefore, some of the results will be exploited via open-source and others via different licensing mechanisms. Some of the results will remain company-confidential and will be exploited by individual partners on the market. This first version of the exploitation plan has been drafted at the end of year 1 of ISOLDE. During this stage initial technical results have been achieved, but technical maturity

still needs to increase. The information in Section 3 of this document supplements exploitation information in Part A and Part B of the Grant Agreement and includes contributions from partners with addenda thereto.

1 Dissemination & Exploitation Objectives

The dissemination and exploitation protocol followed by ISOLDE partners describes the process, conditions, and restrictions for public dissemination and commercial exploitation of project results. The objectives thereby are to reach an as big as possible audience from an R&D perspective as well as from a commercial success story. The ISOLDE and TRISTAN consortia will thereby work closely together in order to be fully aligned on common initiatives and results.

The overall key-message for relevant academic, industrial and societal stakeholders is that “ISOLDE will contribute toward European sovereignty for embedded processors”. Sub-messages to each target group will be refined/modified during the lifetime of the project. The external dissemination and exploitation plan will – in any case – strongly emphasize the importance of allowing stakeholder communities to deliver feedbacks to the project and become involved in the co-design approach for new applications based on RISC-V.

The main dissemination objectives are:

1. Create awareness on ISOLDE primarily in the EU RISC-V ecosystem and in particular about the IP blocks being developed (adoption)
2. Enlarge to non-consortium members the current ecosystem contributing to ISOLDE
3. Enhance the uptake of ISOLDE results into new industrial applications

To achieve these objectives the proposed dissemination and exploitation plan describes the methodology and channels used to address the three target groups as mentioned in the DoA:

(1) companies (both large enterprises and SMEs) who include RISC-V in their designs and products.

(2) universities and RTOs to educate and expand the user community in RISC-V based design.

(3) dissemination and outreach to policymakers, the media and the wider public.

Also new initiatives, e.g., the set-up of new industrial entities, will be envisioned and stimulated through the results obtained in both TRISTAN and ISOLDE.

2 Dissemination and Communication

2.1 Corporate image

To allow an appropriate visibility and recognition of ISOLDE, the consortium has developed a common graphic identity for the project. This corporate image differentiates the project from other initiatives or organizations, and it is reflected in all ISOLDE communications, printed materials, campaigns, websites or simply how the consortium talks about the project. The following subsections reflect the corporate image developed in the project:

Logo

A project logo has been designed with the purpose of communicating feelings related to the technology sector. The logo keeps the same patron as the TRISTAN project to find the relationship between both projects. This logo is the main graphic to represent the project and it is used in all dissemination and communication material.

Templates

A set of designed templates are used to maintain the corporate image of the project:

- **Presentation template (PPT):** All partners use the presentation template for their internal (e.g., General Assemblies or WP-specific meetings) and external presentations (e.g., conferences, workshops, B2B meetings). The file is stored in the ISOLDE repository for use by all partners in creating standard layouts, font sizes, etc. This template is designed in 16:9 format in Microsoft Office PowerPoint and it also includes the EC disclaimer, as well as all partners' logos. Additionally, the consortium has an official presentation which synthesizes the project in a few slides and can be used as generic presentation and info-set for the whole consortium.



Figure 1: ISOLDE PPT template

- **Deliverable template (DOC):** To ensure uniformity among all the documents submitted to the European Commission, a template with a standard format has been created. This template is available for usage by partners in Microsoft Office Word and it is also available on the consortium repository.

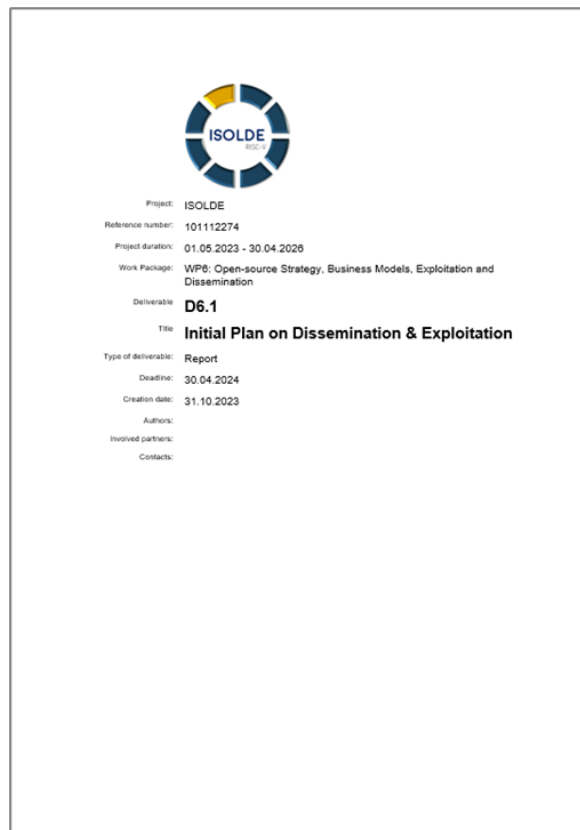


Figure 2: ISOLDE deliverable template

2.2 Website

The ISOLDE website (<http://www.isolde-project.eu/>) plays a key role in the dissemination task as the primary channel to get information about the project. The site provides general information about ISOLDE, includes updated pieces of news and grants the communication of the consortium with different audiences.



Figure 3: Home page of the ISOLDE website

The website of the project was designed by edacentrum, who is supporting the project consortium and the project coordinator in managing, maintaining and editing the content of it, as well as providing the corresponding statistics.

The Matomo monitoring tool has been implemented to obtain relevant information about the audience and drive better decisions regarding its contents, if necessary, to ensure the effectiveness of the site. As of April 2024, the website has obtained a total of 2.603 visits.

After modifications, the menu of the website is currently composed by a “Home” page and the following sections:

– PUBLIC AREA:

- Project profile: it contains a definition of the project.
- Project partners: this section reviews the partners of the consortium, including their logo and their websites.
- Publications: it contains any open-access peer-reviewed publication related to the project.

- LinkedIn: to show interconnectivity between all dissemination tools, the LinkedIn profile link is included here.
- Privacy Policy: it redirects to the edacentrum Data Protection Declaration information for users.
- Imprint: it includes relevant material for users which can be used publicly.
- PRESS:
 - News: this section includes all news developed by the consortium with continuous updates of the project.
 - Press review: it includes press clippings of the project.
 - Press releases: material for press is included here with relevant information from project updates.
- INTERNAL AREA:
 - Login/register: this is the way of accessing the consortium-restricted area for partners, in which information available from the internal repository is included.

The launch of the website was in project M3 and since then it is regularly kept updated with technical and non-technical news about the project in the News section. To achieve that, FENTISS, as task leader of the dissemination and communication task, created an editorial plan based on contributions from all partners.

In this reporting period, the website has included 9 contributions including technical and non-technical pieces of news, which helped in the increase of content to improve SEO performance¹ and to boost the traffic on the website.

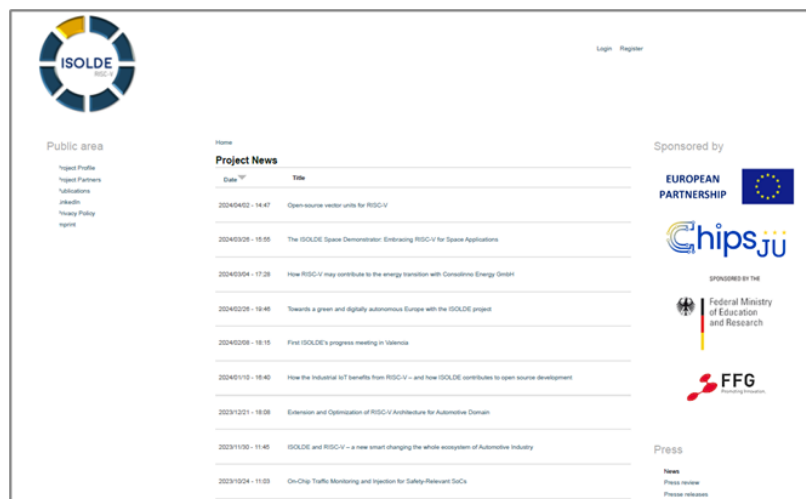


Figure 4: News section in the ISOLDE website

¹ SEO performance stands for how well a website ranks on search engines (like Google) and attracts organic traffic



Figure 5: Example of a piece of news in the ISOLDE website

These contributions are managed by FENTISS through an editorial plan created for all partners with available efforts on T6.2. The consortium follows an exhaustive process for content creation, which implies that each partner with effort in T6.2 shares in a common document the plan of action in the forthcoming quarters. This document is available on the repository with open topics for partners to allow some flexibility on the development that each partner wants to communicate.

EDITORIAL PLAN ISOLDE			
Month	Title	Partner	Status
Sept - Oct 23	ISOLDE and RISC-V -a new smart changing the whole ecosystem of Automotive Industry	BEIA	POSTED (11/23)
	On-chip traffic monitoring and injection for safety-relevant SoCs	BSC	POSTED (10/23)
Nov - Dec 23	Extension and Optimization of RISC-V Architecture for Automotive Domain	BUT	POSTED IN DECEMBER
	How the Industrial IoT benefits from RISC-V – and how ISOLDE contributes to open source development	BYK	POSTED IN JANUARY
ene-24	Towards a green and digitally autonomous Europe with the ISOLDE project	CODA	POSTED IN FEBRUARY
feb-24	How RISC-V may contribute to the energy transition with Consolinno Energy GmbH	CONSOLINNO ENERGY	POSTED IN MARCH
	The ISOLDE Space Demonstrator: Embracing RISC-V for Space Applications	E4	POSTED IN MARCH
March 24	Open-source vector units for RISC-V	ETHZ	POSTED IN MARCH
	Leveraging RISC-V systems' safety by using hypervisors	FEN	Ready to review (post in April)
abr-24	Simulation support in a generator driven RISC-V design flow	FZI	Ready to review (post in April)
		GSL	
May 24		HM	
		IFX	
June 24		IMT	
		POLIMI	
jul-24		LDO	
		NXP-AT	
ago-24		NXP-CZ	
		OFFIS	
sep-24		POLIMI	
		RAPITA	
Oct 24		SAL	
		SILVACO	
nov-24		SYSCO	
		TASI	
Dec 24		TRT	
		TUI	
		UNIBO	

Figure 6: Internal document for the editorial plan

The editorial plan follows an exhaustive process for its publication, with 2 posts monthly. Partners whose contribution is expected (according to the plan) receive an email to choose a

technical topic and provide a piece of news at the end of the month. Once the task leader receives these two contributions, this person sends an email to the WP6 collaborators to review this contribution, make any edits or provide some feedback in the following two weeks. After this review period, the task leader finally approves the contribution and sends the final text with a thumbnail image and all the additional details in terms of design and add-ons to the webmaster in the following days, who uploads these posts accordingly to the website. This process allows all members of the consortium to be involved in this activity and provides additional feedback to get the most adequate information which fits with all partners' expectations. The results of the editorial plan are quite satisfactory, providing enough content to keep the website updated as well as to share it on social media.

2.3 Social Media

Social media is a key aspect of the dissemination strategy for increasing distribution efforts and involving part of the target audience of the project. Due to the professional nature of the project, WP6 leader has chosen LinkedIn as the main social media platform.

ISOLDE's social media strategy consists of creating content which helps to increase traffic to the website, as well as engaging the community through the influence of the consortium partners' profiles.

As of April 2024, the LinkedIn profile of the project has 137 followers obtained through the spread of word of the project and thanks to the pieces of news shared in the profile and in the partners' profiles.

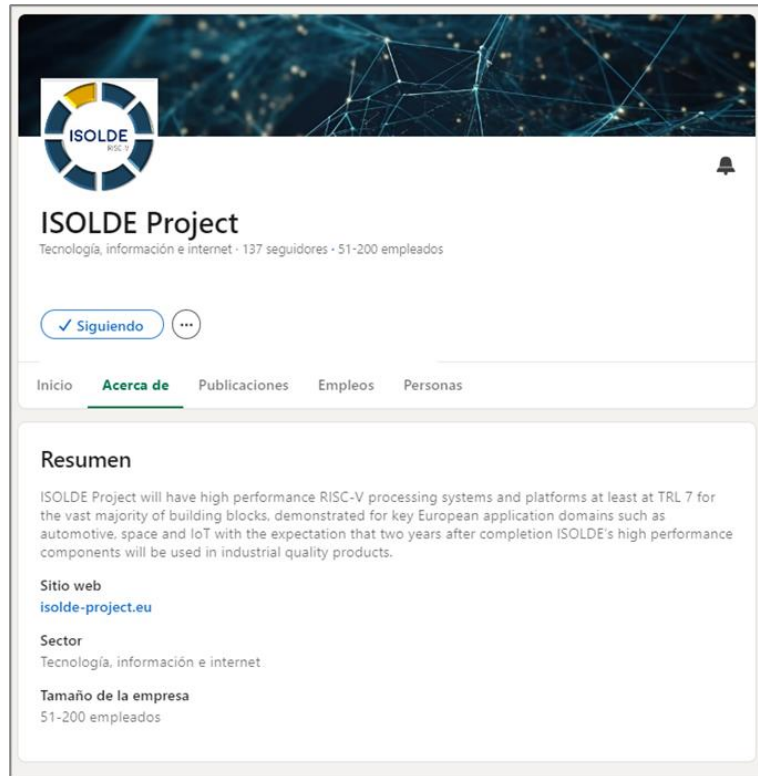


Figure 7: ISOLDE's LinkedIn profile

2.4 Dissemination and communication materials

As of April 2024, ISOLDE has available a poster with some information about the project to be used by partners. This poster design represents a useful piece of material for partners for those conferences in which there are poster exhibitions, and it can also serve as a good resource for easily explaining the project overview to an audience in any face-to-face event. Additionally, the consortium is currently designing a joint flyer with the TRISTAN project to give visibility to both projects and show the collaboration between both initiatives.

Last not least, an official presentation of the ISOLDE project has been approved by all partners with content that may be shared to easily disseminate the goals and activities carried on in the project.

2.5 Events

Participation to events plays a crucial role in the success of the dissemination strategy of ISOLDE, serving as effective platforms for successful communication and engagement. These events offer unique opportunities to disseminate project outcomes, share knowledge, and foster collaborations among stakeholders. They provide a space for partners, policymakers, researchers, and industry experts to gather, exchange ideas, and showcase their

achievements, raising awareness about the objectives and results of the project and creating a wider impact by reaching a diverse audience.

As of April 2024, the consortium has participated in a total of 18 events:

Date	Event	Location	Partner	Description	Target audience
January 2023	MCS: Mixed Critical Systems – Safe and Secure Intelligent CPS and the development cycle	Toulouse, France	BSC	Presentation at the "MCS : Mixed Critical Systems – Safe and Secure Intelligent CPS and the development cycle" Workshop by Jaume Abella (BSC): "Open Source HW for Safety-Critical Systems in Europe". ISOLDE project introduced as part of the talk	Research communities
June 2023	ADTC 2023	Grenoble, France	SYSGO	Presentation "A view on RISC-V research from dependable operating systems" at ADTC 2023 Grenoble "Technical Session: RISC-V"	Research communities
June 2023	Dataweek 2023	Luleå, Sweden	INTEL	Organization of the Track "RISC-V: an opportunity for the European R&I&D ecosystems", where TRISTAN and ISOLDE (see below) presentations were provided. A Panel was run at the end, involving Track invited speakers and Daniel Opalka, (Head of R&I at European HPC JU) This was the first joint dissemination activity among the two projects.	Industry / Research communities
June 2023	Dataweek 2023	Luleå, Sweden	IFX	Presentation of the project in the Dataweek 2023 – Data meets Infrastructure at the Edge titled "ISOLDE - High Performance, Safe, Secure, Open-Source Leveraged RISC-V Domain-Specific Ecosystems"	Industry / Research communities

September 2023	ORConf 2023	Munich, Germany	HM	HM organized the leading open source silicon conference at HM. Various partners presented.	Other
September 2023	OpenEMS workshop	Göttingen, Germany	SYSGO	SYSGO participated in OpenEMS workshop (to better learn OpenEMS for Task 5.3 work) and also introduced RISC-V work and ISOLDE to workshop participants	Industry/ business partners
September 2023	French Space Agency and Airbus Defence and Space FR	Toulouse, France	FEN	Presentation to the French Space Agency and Airbus Defence and Space FR, both located in Toulouse	Specific end user communities
October 2023	RVF (RISC-V FW) workshop	Tampere, Finland	SAL	Presentation at the RVF (RISC-V FW) workshop in October 2023 in Tampere, Finland by Andrew Wilson (SAL)	Research communities
October 2023	RVF (RISC-V FW) workshop 2023	Tampere, Finland	IFX, TAU, TUM, EDA	Co-Organization of the RVF (RISC-V FW) workshop 2023	Research communities
November 2023	RISC-V Summit North America 2023	Santa Clara, California	HM	HM presented a poster on ISOLDE	Other
November 2023	Super Computing Conference 2023	Denver, USA	E4	E4 participated as a speaker in the Second International Workshop on RISC-V for HPC.	Research communities
November 2023	Future of Compute/VC Dinner	Munich, Germany	HM	HM participated in a VC dinner and represented RISC-V and European research	Investors
January 2024	HPC Asia	Nagoya, Japan	E4	Talked about ISOLDE regarding the E4 Experience with RISC-V in HPC	Research communities
March 2024	Acatech	Germany	HM, IFX	HM and IFX participated in the discussions and contributed to a report for the German federal public bodies.	National authorities

March 2024	Multicore MACH 178 Training workshop	Noordwijk, Netherlands	RAPITA	Delivered part of a specialized training course on the multicore technologies to future customers. Held in the European Space Agency - European Space Research and Technology Center	Specific end user communities
April 2024	ADTC 2024	Dresden, Germany	HM	HM presented on current RISC-V research activities and how they evolve to platforms: "RISC-V and Europe in 2024"	Research communities
April 2024	Rohde + Schwarz Internal Developer Conference 2024	Munich, Germany	HM	HM presented the basics of RISC-V along with an overview of European research activities	Industry/business partners
April 2024	Multicore MACH 178 Training workshop	Madrid, Spain	RAPITA	Delivered part of a specialized training course on the multicore technologies to future customers	Specific end user communities
April 2024	Hannover Messe 2024	Hannover, Germany	BYK	Showcased the prototype to deploy smart home adapters to resource-constrained edge devices	Industry/business partners

Table 1: ISOLDE's list of events

The consortium has closely collaborated to disseminate ISOLDE among different appointments and diverse audiences. Additionally, the consortium already has plans for several other events in the following months.

2.6 Publications

As of April 2024, the consortium has participated in 5 publications following the open-science rules from the European Commission, all these coming from conference proceedings:

Title	Title of the journal /or equivalent	Date	Authors	Link
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SafeLS: An Open Source Implementation of a Lockstep NOEL-V RISC-V Core	IEEE 29 th International Symposium on On-Line Testing and Robust System Design (IOLTS), 2023	July 2023	M. Sarraseca, S. Alcaide, F. Fuentes, J.C. Rodriguez, F. Chang, I. Lasfar, R. Canal, F.J. Cazorla, J. Abella (BSC)	here
Black-Box IP Validation with the SafeTI Traffic Injector: A Success Story	IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2023	Oct 2023	F. Fuentes, S. Alcaide, R. Casanova, J. Abella (BSC)	here
RISC-V Processor Technologies for Aerospace Applications in the ISOLDE Project	International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS) 2023 conference	July 2023	W. Fornaciari, F. Reghenzani, G. Agosta, D. Zoni, A. Galimberti, F. Conti, Y. Tortorella, E. Parisi, F. Barchi, A. Bartolini, A. Acquaviva, D. Gregori, S. Cagnetta, C. Ciancarelli, A. Leboffe, P. Serri, A. Burrello, D. Jahier Pagliari, G. Urgese, M. Martina, G. Masera, R. DiCarlo, A. Sciarappa (POLIMI, UNIBO, E4, TASI, POLITO, LDO)	here
MX: Enhancing RISC-V's Vector ISA for Ultra-Low Overhead, Energy-Efficient Matrix Multiplication	Design Automation and Test in Europe (DATE) Conference 2024	Mar 2024	M. Perotti, Y. Zhang, M. Cavalcante, E. Mustafa, L. Benini (ETHZ, UNIBO)	here
The European Chips Act, The ISOLDE Project, and Open-Source Hardware	Argentine Conference on Electronics (CAE)	Mar 2024	Willibald Krenn, Andrew Wilson, Ambily Suresh, Manuel Freiberger (SAL)	here

Table 2: ISOLDE's list of publications

In addition to this, the consortium has also submitted a few abstracts for some conference proceedings which will be reported in the next update of the current document in case those will be accepted.

2.7 Collaboration with other initiatives

By forging partnerships with other related projects, organizations, and initiatives, ISOLDE can leverage collective knowledge, resources, and expertise to achieve its objectives more efficiently. Collaborative efforts enable the project to achieve synergies to address common challenges and enhance the visibility of the project.

ISOLDE's partnership with other EC-funded projects has been mainly focusing on the collaboration with the TRISTAN project. The scientific approach in ISOLDE builds upon a close

collaboration with TRISTAN and aims at a clear path towards industry qualification of RISC-V based IP to enable the adoption of many open-source hardware IPs at an industrial level.

The consortium constantly monitors the different initiatives and projects which can promote mutual learning and innovation, which, jointly with partners' broad experience and participation in H2020 and HE projects, can create opportunities to find these collaborations soon. Currently, the ISOLDE project is member of the following initiatives:

- **RISC-V International:** this is a global non-profit association based in Switzerland. Founded in 2015 as the RISC-V Foundation with 29 members, RISC-V is now a truly global organization with over 200 member organizations in more than 30 countries, plus over 300 individual members worldwide. The RISC-V Foundation was founded to build an open, collaborative community of software and hardware innovators based on the RISC-V Instruction Set Architecture (ISA). The consortium has been a member of this network since August 2023.
- **Open-source initiative:** this is a non-profit corporation with global scope formed to educate about and advocate for the benefits of open-source and to build bridges among different constituencies in the open-source community. Open-source enables a development method for software that harnesses the power of distributed peer review and transparency of process, something that fits in the scope of the ISOLDE project.

2.8 Other communication activities by partners

Apart from the activities mentioned above, the consortium has also been active in the communication of the project in other aspects. With a total of 32 partners participating in this task, the whole consortium has also introduced the project in other types of occasions which are reflected in the following lines differentiating between digital channels and face-to-face presentations.

On digital channels

Digital channels play a key role in the communication activities of all members of the consortium. Some partners have decided to make use of these mechanisms to present the project to their specific followers or users:

- Presentation & information of the project on RAPITA's website & LinkedIn (July 2023): <https://www.rapitasystems.com/news/rapita-proud-be-isolde-partner>

- https://www.linkedin.com/feed/update/urn:li:activity:7089549794188124160?updateEntityUrn=urn%3Ali%3Afs_feedUpdate%3A%28V2%2Curn%3Ali%3Aactivity%3A7089549794188124160%29
- Post at RAPITA's LinkedIn (April 2024):
https://www.linkedin.com/feed/update/urn:li:activity:7189169512527581185?updateEntityUrn=urn%3Ali%3Afs_feedUpdate%3A%28V2%2Curn%3Ali%3Aactivity%3A7189169512527581185%29
- Blog post on Bytefabrik's website: <https://bytefabrik.ai/en/blog/2023-07-08-kickoff-isolde/>
- Blog post on CODASIP's website: <https://codasip.com/2023/12/20/isolde-towards-a-green-and-digitally-autonomous-europe/>
- Information of the project on FENTISS' website: <https://www.fentiss.com/eu-funded-projects/>

Face-to-face presentations

Partners have been able to present the project on several occasions during private meetings, business trips or during networking activities. Here below some examples:

- Business presentations from FENTISS: FENTISS presented the project in September 2023 to Airbus Defence and Space and the French Space Agency (CNES) during a business trip to Toulouse.
- Presentation to CDTI from FENTISS: FENTISS presented the project to the Spanish Center for Technological Development and Innovation (CDTI).
- Presentation to UPV students: Due to the research nature of FENTISS and the strong connection between the company with the UPV, FENTISS presented the project in the Master's Degree in Computer and Network Engineering of the UPV university.

2.9 Key Performance Indicators (KPIs)

To facilitate an accurate monitoring and assessment of the accomplished communication and dissemination activities, and to understand the impact of the actions carried out, all partners register the implemented activities on a common file. This document is a shared Excel file available on the common repository to report every communication- and dissemination-related activity or publication made by each consortium member. Thanks to it, the consortium can report the advancements of this task in the most complete way.

Additionally, the consortium has also developed a set of Key Performance Indicators (KPIs) to report the performance of communication and dissemination activities. By performing regular

monitoring of the activities, it is possible to assess whether the action plan is being carried out properly.

As of April 2024, the progress of the KPIs is as follow:

METRIC	DETAILS	KPI	Progress M12
Graphic identity	Logo in different formats	1	1
	PPT template	1	1
	Word template	1	1
Website	Number of sessions on the website	4000	2603
Social media	Followers on the LinkedIn profile	400	153
Promotional materials	Flyer	1	0
	Poster	1	1
	Project video	1	0
Media liason	Press releases	2	0
	Press clippings	15	0
Participation in events	Number of research and industry events, including conferences booths, workshops, tutorials, etc.	50	18
	Number of joint workshops	1	0
	Total number of participants in workshops	50	0
Publications	Research papers	1	4

Table 3: KPI list and progress

Looking at the previous table, the consortium has had a positive performance in the first year of its duration, starting with the dissemination activities at an initial stage. Activities were focused on the development of a visual identity for ISOLDE, as well as on the setup of the corresponding channels, the creation of content, and the brand awareness of the project between different audiences at several events.

In the following months, the consortium will continue working on the same line, developing better graphic material to disseminate the project uniformly and in the best possible way, as

well as looking for collaborations from partners and synergies with TRISTAN to increase the visibility of ISOLDE.

Therefore, it can be said that ISOLDE has achieved, at the end of the first reporting period, a number of dissemination and communication activities that gives confidence that at project end we will reach - and even go beyond - the project goals according to the commitments of the Grant Agreement.

3 Exploitation

The RISC architecture has emerged as a pivotal force in the semiconductor industry, offering efficiency and flexibility in comparison to Complex Instruction Set Computing (CISC) architectures. RISC-V, an open-source RISC instruction set architecture, has gained substantial attention due to its inherent advantages. Its open nature allows for collaborative innovation, making it an ideal platform for the development of cutting-edge technologies.

RISC-V's modular structure and open-source licensing have fostered a community-driven approach to processor design. This collaborative environment has the potential to revolutionize the industry by encouraging diverse contributions from various stakeholders. The architecture is not only flexible but also highly customizable, making it suitable for a broad range of applications, from embedded systems to high-performance computing.

The semiconductor industry has traditionally been characterized by proprietary designs and closed ecosystems. However, the paradigm is shifting towards open-source methodologies, driven by the success of initiatives like RISC-V. Open-source in the semiconductor domain promotes transparency, knowledge sharing, and accelerated innovation cycles. It enables a broader community to participate in the development process, breaking down traditional barriers and fostering a culture of collaboration. ISOLDE is playing a key role in expanding and maturing the RISC-V ecosystem in Europe, and the exploitation plan proposed in this deliverable provides the direction for the consortium partners to further exploit the results of ISOLDE.

One role of the project demonstrators is to show that the RISC-V ecosystems as a whole is mature enough to run industrially relevant systems. E.g., the smart home demonstrator picks a mature open-source energy management systems (OpenEMS, <https://openems.io/>) and demonstrates that it can be run on the open hardware CVA6² system.

3.1 Open-Source Hardware Exploitation

UNIBO and ETHZ have been contributors to the open-source hardware ecosystem for many years via the academic-driven RISC-V-based PULP Platform³ open-source project, where many of the open-source IPs in ISOLDE have originally been incubated, e.g., CVA6 (originally,

² [CVA6: An application class RISC-V CPU core — CVA6 documentation \(openhwgroup.org\)](#)

³ [PULP FAQs \(pulp-platform.org\)](#)

Ariane). Both UNIBO and ETHZ are exploiting new/improved IPs developed in ISOLDE to boost the EU open-source hardware ecosystem. Specifically, activities carried out in the Space demonstrator will build up on the Cheshire platform (<https://github.com/pulp-platform/cheshire>), contributing back innovation and changes, as well as bug-fixes. UNIBO will utilize RedMule (<https://github.com/pulp-platform/redmule>) and OpenTitan (<https://github.com/lowrisc/opentitan>) and upstream all relevant modification.

BSC's Laboratory for Open Computer Architecture (LOCA) offers a number of IPs in the form of open-source. Those IPs include the SafeSU (<https://github.com/bsc-loca/SafeSU>) and SafeTI (<https://github.com/bsc-loca/SafeTI>), which are being evolved and matured as part of ISOLDE. Those components have already been integrated in a SoC based on GSL technology with NOEL-V cores, which is the primary choice for the automotive use case, so we plan to evaluate those components in the context of that use case.

GSL provides an open-source version of the IP library products of the company (<https://www.gaisler.com/getglib>). The extensions planned in ISOLDE will be disseminated through this library, including cybersecurity extensions and the added functionality to interface the VPU from partner ETHZ.

E4 Computer Engineering predicted several outcomes for the exploitation. First of all the know-how acquired by E4 in the ISOLDE project will apply to any market or industry sector where the RISC-V ISA may provide an answer to the requirements for openness; it is also expect the design of accelerators that can be integrated into the processor design and an architectural design based on CV6A, as well as visibility in the RISC-V environment.

TRT contributes to the open-source hardware community via the OpenHW Group⁴, particularly through the development of the CVA6 cores (<https://github.com/openhwgroup/cva6>), and the participation at the RISC-V International. The Context-Aware Monitoring infrastructure developed in ISOLDE will be based on CVA6 designs, contributing back innovation, changes and bug-fixes to those designs.

HM develops bytecode virtualization extensions, that are prototypically implemented in state-of-the-art open-source RISC-V cores. The extensions are designed in a modular and

⁴ [OpenHW Group | OpenHW Group](#)

composable way, and their integration will be released as forks of the GitHub organization of the lab (<https://github.com/hm-aemy/>), while some parts of the work will be contributed to upstream processors in discussion with the project maintainers.

3.2 Open-Source Software Exploitation

The FZI contributed to the Linux release 6.8 (<https://riscv.org/news/2024/01/risc-v-with-linux-6-8-restores-xip-kernel-support/>) by restoring the eXecute In-Placement (XIP) functionality for RISC-V. XIP enables the Linux kernel to “execute in place” from ROM without copying into RAM. The work is intended to support one envisioned safety mechanism in future work within ISOLDE. This way ISOLDE fosters RISC-V support in Linux.

The founders of BYK are the original creators of Apache StreamPipes (<https://streampipes.apache.org>), a top-level project of the Apache Software Foundation (ASF) for industrial data analytics. Today, Apache StreamPipes has evolved to a large community-driven open-source project with the source code available at <https://github.com/apache/streampipes>. To date, BYK still provides the majority of developer resources to that open-source project. As such, substantial results developed within ISOLDE (especially concerning management of edge nodes and selective adapter deployment to resource-constrained edge devices) are contributed to the open-source project on a regular basis. In addition, smart home adapters developed within WP5 are also fully integrated into the open-source project. It is expected that the first official release containing technical results developed within ISOLDE will be version 0.97.0. The open-source code developed within ISOLDE follows the standardized and quality-oriented ASF development process.

3.3 Open-Source Tool Exploitation

HM is a contributor to Verilator (<https://github.com/verilator/verilator/>). Smaller contributions have been merged into the project already. The main work of the ISOLDE project (instrumentation support) is on track.

3.4 Company-specific (non open-source) Exploitation

Development of the AI/ML accelerator and its integration with the RISC-V host CPU gives FotoNation considerable leverage to develop its next generation of AI hardware accelerator; these are designed to have enhanced support for new AI operators, be faster and more power efficient, with less integration size used.

The ISOLDE project enables FotoNation to further advance its understanding of RISC-V ecosystem consisting of CPU, memories, accelerators, SW tools and how to best utilize these in its next generation of AI / ML driven products. FotoNation's multiple industries (digital still camera, mobile phone) proven ML and neural imaging solutions will be the key differentiator for its next generation hardware accelerated, low power and computationally efficient edge-based technologies. Such imaging solutions have already become a critical technology for mobile device manufacturers and are poised to be widely adopted in other industries including automotive, surveillance and home monitoring.

One of FotoNation core competency is the ability to provide solutions implemented as either highly optimized software only implementations or hybrid implementations (SW with hardware Image Processing Unit (IPU) based acceleration). FotoNation's experience to enable the target silicon platforms to optimally execute image processing algorithms via its IPU is one of the main differentiations. Its next generation of RISC-V enhanced IPU will be a new processing paradigm, proven in other markets, geared towards specialized image processing computing and AI on the edge, where real-time response is required.

To promote and to gain awareness of the results achieved through the ISOLDE project, FotoNation will organize at least one workshop with potential customers. The company will also participate in at least one conference or congress to increase its visibility and encourage broader scale adoption of the results.

Space demonstrator activities carried out within the ISOLDE project align with Thales Alenia Space Italy (TASI) internal Earth Observation roadmap for deploying innovative AI-based solutions on board new generation LEO satellites. TASI recognizes the increasing significance of AI in space systems and the importance of efficient hardware and software solutions for enabling edge processing. By utilizing the flexibility and scalability of RISC-V, TASI can integrate specialized hardware acceleration for AI algorithms, improving computational efficiency for critical on-board functions, such as satellite health monitoring. The open-source nature of RISC-V also enables easy customization to meet specific mission requirements.

One of the FENTISS' objectives in this project is to port the CVA6 processor into the XtratuM Hypervisor to enlarge the portfolio of supported processors, particularly targeting the space industry. This processor holds great potential due its ability to support intensive workloads and its reliability in critical environments. The addition of this processor to the portfolio of XtratuM

hypervisor expands the potential market and offers an opportunity for growth and collaboration in the space industry.

FENTISS is collaborating with other partners like RAPITA, GSL, BSC and UPV:

- Rapita offers various Timing Analysis tools utilized in hypervisors. FENTISS will support the Timing Analysis Tools from RAPITA in their XtratuM hypervisor. This collaboration enables users of Rapita tools to access a broader range of options and consider FENTISS' hypervisor, as well as XtratuM users having access to more compatible timing tools.
- Another partner FENTISS will be working with is GSL. Currently XtratuM supports RISC-V with NOEL-V, but GSL will be making improvements to their processor in order to update to new RISC-V specifications and standards. The system software needs to keep up with these new processor developments and standards. Keeping up to date to support new updates is vital to ensure the compatibility, quality and relevance of FENTISS' software in critical markets.
- Another partner that FENTISS will be working with is BSC to support their SafeSU and SafeTI units in the XtratuM hypervisor, improving the observability and stress of the system. This collaboration allows users of SafeSU and SafeTI to observe and stress the system running XtratuM.
- FENTISS will also work with UPV to integrate their fault injection testing tool, as required by automotive industry standards. This integration will allow FENTISS to support this tool seamlessly and transparently to the user. In addition, this collaboration serves as a pathway for FENTISS to enter new markets such as the automotive industry, potentially expanding its reach and business opportunities.

Rapita Systems provides on-target software verification tools and services globally to the embedded aerospace and automotive electronics industries. Rapita contributes to ISOLDE with the development of its MACH-178 solution⁵ for the selected RISC-V architectures for the Automotive and Space domains. MACH-178 is aimed at enabling the certification of multicore System-on-Chips in the avionics, space and automotive domains regarding timing safety.

⁵ [MACH178 | Rapita Systems](#)

Work on ISOLDE will result in a first addition of RISC-V-based architectures into the MACH-178's portfolio of supported SoCs. Rapita presence in the RISC-V landscape allows to have direct interaction with potential customers using RISC-V multicore SoCs, in application domains needing to certify their applications for timing safety.

Rapita is currently working on licensing terms for its solution, in collaboration with its sales partner Rapita Systems, Ltd (UK).

SYSGO plans to use ISOLDE results on multicore PikeOS RISC-V for supporting future developments in the RISC-V market. The contribution in the planned demonstrations in smart home and satellites help to position SYSGO with a strong portfolio in RISC-V.

CONS plans to strengthen the portability of its energy management platform through doing the RISC-V and i.MX8 porting. Moreover, the reason for migration to i.MX8 is the need for more computing power (e.g., for strong optimization algorithms) thus positioning us better on the future markets. CONS also foresees to be well-positioned for any powerful in-silicon RISC-V application processor or SoC once there are attractive offerings for this for our embedded system market needs.

IMT is working with the Romanian Universities, Research Institutes and companies to promote open-source hardware and the RISC-V ecosystem. Some Romanian Universities are already planning on migrating some of their computer architecture courses to teach the RISC-V architecture. Furthermore, in the next editions of the “Technologies of Interconnections in Electronics” (<https://tie.ro/>) event we plan on evaluating the impact of open-source hardware and RISC-V from the perspective of advanced packaging and chiplets. This year we had in Sibiu, Romania the first edition of the TIE Micro competition which aims to introduce students to these advanced packaging techniques.

INTEL is collaborating with the three project partners (Tobii, IMT, and Silicon Austria) that declared interest to the Intel shuttle Program and is granting them access to the Intel shuttle Program toolkit, allowing ISOLDE partners to deep dive into Chip design considerations (design constraints, tool-flow, KPIs, ...) with the aim to increase European ecosystem awareness and expertise of recent technology nodes design.

Besides the aforementioned open-source contributions to Apache StreamPipes, Bytefabrik aims to extend its commercial product portfolio with custom algorithms and user-faced plugins related to the Smart Home use case. While the technological foundation for dynamic adapter deployment will be part of the open-source software, additional features supporting larger-scale deployments will be included into commercial plugins. In addition, Bytefabrik also aims at exploiting the open-source results commercially by offering workshops, training and custom services.

GSL brings the extensions made to the NOEL-V processor within ISOLDE directly to the company's NOEL-V product. The VPU interfacing work done within ISOLDE will also benefit future generation multi-processor space-grade SoC products (the sixth generation European space processors⁶).

⁶ [Thales alenia space 6th generation digital transparent processor \(DTP6G\) - a multi-mission, multi-mode versatile product at the heart of telecom solutions | IET Conference Publication | IEEE Xplore](#)

4 Resources & Management

The WP6 core team (WP-leader and Task leaders) is responsible for the development and updates of the dissemination and exploitation plan and for the monitoring of the activities. It also facilitates and monitors specific dissemination and exploitation activities by all partners. Almost all ISOLDE partners are part of WP6 and to that extent are expected to actively participate and deliver dissemination and exploitation activities as/when needed. This includes events, but also contributions to the project website, newsletters and social media. It also includes contributions to standardization. In the first 6 months of the project, the activities have been aimed at installing the basic needs, instructions, guidelines and tools to facilitate dissemination and exploitation in a successful way. Regular alignments will be planned with the TRISTAN project in order to share experiences and best practices and to guarantee a similar reporting structure. In M12 we will start with more externally intensive dissemination and exploitation activities on behalf of the consortium. The dissemination and exploitation teams will meet at least every 3 months. This will ensure that all interests are reflected by the activities and contains a shared responsibility in the success thereof.

In YR2 of ISOLDE, the first demonstrators will become available, meaning that the dissemination and exploitation teams will be extended with representatives from WP5. As from that moment the frequency of the dissemination and exploitation team meetings will be increased to at least every 2 months.

5 Conclusion

The open-source approach of TRISTAN and ISOLDE makes the importance of proper dissemination and exploitation of project results even more important. Dissemination and exploitation activities raise the visibility of open-source projects and the contributors. By sharing project updates, research findings, and success stories, both projects will gain recognition within the relevant communities and industry sectors. This visibility can attract new collaborators, users, funding opportunities, and potential partnerships. It will allow anyone, regardless of their background or affiliation, to access project information, contribute to its development, and benefit from the outcomes of the project. Dissemination and exploitation ensure that valuable knowledge and innovations are not restricted to a select few but are available to the broader public.

TRISTAN and ISOLDE have implemented a stepped dissemination and exploitation approach, from organising the basic infrastructure, tools, templates and way of working, to more intensified team effort toward dissemination and exploitation. By using well-established channels, networks, and events we are able to reach out to the relevant stakeholders and generate significant impact in the RISC-V ecosystem.

This first ISOLDE exploitation plan clearly indicates the great commercial and academic potential of the project for its project partners. This plan outlines a comprehensive approach to ensure that ISOLDE not only delivers technological innovation but also contributes positively to the ecosystem, adaptation of RISC-V, communities, and the overall well-being of the open-source Semiconductor industry.

In M24 and M36 updates of this plan will be provided, detailing the results to that date but also providing more insights in the scale and impact of the exploitation efforts.